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Applicants: William T. CHEN, et al.)
Serial No.: 10/029,435)
Filed: December 18, 2001) Our Ref: B-4361 61-9
For: "METHOD OF FORMING SELECTIVE)
ELECTROLESS PLATING ON...") Date: March 20, 2002

CLAIM TO PRIORITY UNDER 35 U.S.C. 119

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

[X] Applicant hereby makes a right of priority claim under 35
U.S.C. 119 for the benefit of the filing date(s) of the
following corresponding foreign application(s):

<u>COUNTRY</u>	<u>FILING DATE</u>	<u>SERIAL NUMBER</u>
SINGAPORE	19 December 2000	200007713-1


[] A certified copy of each of the above-noted patent
applications was filed with the Parent Application
No. _____

[X] To support applicant's claim, a certified copy of the above-
identified foreign patent application is enclosed herewith.

[] The priority document will be forwarded to the Patent Office
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I hereby certify that this correspondence
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Respectfully submitted,


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This is to certify that the annexed is a true copy of the following Singapore patent application as filed in this Registry.

Date of Filing : 19 DECEMBER 2000

Application Number : 200007713-1

Applicant(s) : INSTITUTE OF MATERIALS RESEARCH
AND ENGINEERING

Title of Invention : METHOD OF FORMING SELECTIVE
ELECTROLESS PLATING ON PLOYMER
SURFACES

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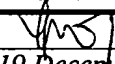
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200007713-1

REQUEST FOR THE GRANT OF A PATENT
THE GRANT OF A PATENT IS REQUESTED BY THE UNDERSIGNED ON THE BASIS OF THE PRESENT APPLICATION

I Title of Invention	METHOD OF FORMING SELECTIVE ELECTROLESS PLATING ON POLYMER SURFACES			
II Applicant(s) (See note 2)	(a) Name	INSTITUTE OF MATERIALS RESEARCH & ENGINEERING		
	Body Description/ Residency	A Public company incorporated under the laws of Singapore		
	Street Name & Number	No. 3, Research Link		
	City			
	State			
	Country	Singapore 117602		
	(b) Name			
	Body Description/ Residency			
	Street Name & Number			
	City			
	State			
	Country			
	(c) Name			
	Body Description/ Residency			
	Street Name & Number			
City				
State				
Country				
III Declaration of priority (See note 3)	Country/Country Designated		File No	
	Filing Date			
	Country/Country Designated		File No	
	Filing Date			
	Country/Country Designated		File No	
Filing Date				

IV Inventors (See note 4) (a) The applicant(s) is/are the sole/joint inventor(s) (b) A statement on Patents Form 8 is/will be furnished	<table border="0"> <tr> <td><input type="checkbox"/></td> <td>Yes</td> <td><input checked="" type="checkbox"/></td> <td>No</td> </tr> <tr> <td><input checked="" type="checkbox"/></td> <td>Yes</td> <td><input type="checkbox"/></td> <td>No</td> </tr> </table>			<input type="checkbox"/>	Yes	<input checked="" type="checkbox"/>	No	<input checked="" type="checkbox"/>	Yes	<input type="checkbox"/>	No
<input type="checkbox"/>	Yes	<input checked="" type="checkbox"/>	No								
<input checked="" type="checkbox"/>	Yes	<input type="checkbox"/>	No								
V Name of Agent (if any) (See note 5)	Yeo Wong & Thian										
VI Address for Service (See note 6)	Block/Hse No	78	Level No	32							
	Unit No/PO Box	00	Postal Code	079120							
	Street Name	Shenton Way									
	Building Name										
VII Claiming an earlier filing date under section 20(3), 26(6) or 47(4). (See note 7)	Application No										
	Filing Date										
	<p>[Please tick in the relevant space provided]:</p> <p>() Proceeding under rule 27(1)(a). Date on which the earlier application was amended = or _____</p> <p>() Proceeding under rule 27(1)(b).</p>										
VIII Invention has been displayed at an International Exhibition (See note 8)	<table border="0"> <tr> <td><input type="checkbox"/></td> <td>Yes</td> <td><input checked="" type="checkbox"/></td> <td>No</td> </tr> </table>				<input type="checkbox"/>	Yes	<input checked="" type="checkbox"/>	No			
<input type="checkbox"/>	Yes	<input checked="" type="checkbox"/>	No								
IX Section 114 requirements (See note 9)	<p>The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty.</p> <table border="0"> <tr> <td><input type="checkbox"/></td> <td>Yes</td> <td><input checked="" type="checkbox"/></td> <td>No</td> </tr> </table>				<input type="checkbox"/>	Yes	<input checked="" type="checkbox"/>	No			
<input type="checkbox"/>	Yes	<input checked="" type="checkbox"/>	No								
X. Check List (To be filled in by applicant or agent)	A. The application contains the following number of sheet(s):-										
	1. Request	3	sheets								
	2. Description	9	sheets								
	3. Claim(s)	3	sheets								
	4. Drawing(s)	3	sheets								
	5. Abstract	1	sheets								
	B. The application as filed is accompanied by:-										
	1. Priority document										
	2. Translation of priority document										
	3. Statement of Inventorship & right to grant										
	4. International Exhibition Certificate										
XI. Signature(s) (See note 10)	Applicant (a)										
	Date	19 December 2000									
	Applicant (b)										
	Date										
	Applicant (c)										
	Date										

19 DEC 2000

NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the prescribed fee and 3 copies of the description of the invention, and of any drawings.
2. Enter the name and address of each applicant in the spaces provided at paragraph II. Names of individuals should be indicated in full and the surname or family name should be underlined. The names of all partners in a firm must be given in full. The place of residence of each individual should also be furnished in the space provided. Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided. Where more than 3 applicants are to be named, the names and address of the fourth and any further applicants should be given on a separate sheet attached to this form together with the signature of each of these further applicants.
3. The declaration of priority at paragraph III should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under the Patents (Convention Countries) Order] should be identified and the name of that country should be entered in the space provided.
4. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph IV should be completed by marking the "YES" Box in the declaration (a) and the "NO" Box in the alternative statement (b). Where this is not the case, the "NO" Box in declaration (a) should be marked and a statement will be required to be filed on Patents Form 8.
5. If the applicant has appointed an agent to act on his behalf, the agent's name should be indicated in the spaces available at paragraph V.
6. An address for service in Singapore to which all documents may be sent must be stated at paragraph VI. It is recommended that a telephone number be provided if an agent is not appointed.
7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified at paragraph VII and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(a), they should also indicate the date on which the earlier application was amended.
8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the "YES" Box at paragraph VIII should be marked. Otherwise the "NO" Box should be marked.
9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depositary authority under the Budapest Treaty, then the "YES" Box at paragraph IX should be marked. Otherwise the "NO" Box should be marked.
10. Attention is drawn to rules 90 and 105 of the Patent Rules. Where there are more than 3 applicants, see also Note 2 above.
11. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least 2 months after the application has been filed in Singapore.

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Application Filing Date : / /
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Method of forming selective electroless plating on polymer surfaces

This invention relates to the plating of polymer surfaces and, in particular, to the metallisation of printed circuit boards and flexible substrates.

The Applicant has already proposed a method of selectively plating an aromatic polymer surface comprises illuminating the polymer surface with a laser light to activate desired regions of the surface to be provided with metallisation. When the surface is subsequently immersed in a plating solution, selective seeding occurs on the regions of the polymer surface that have been activated by the laser and metal is deposited on the surface in the desired pattern. Whilst this method is effective in achieving plating of the selectively activated areas, it is found that some seeding, and consequently some plating, occurs outside the activated regions of the polymer surface. In an attempt to minimise this undesired effect, it has been proposed to dilute the seeding solution with water but this does not entirely eliminate the formation of plating in the non-activated areas. As a result, it is difficult to use the prior method in industrial applications.

The present invention aims to provide a plating method which overcomes the disadvantages of the known method and is suitable for use in industrial applications.

Accordingly, in one aspect, the present invention provides a method of plating a substrate material, which when activated by laser light adsorbs seeding particles for an electroless plating process, comprising: applying a strippable coating to a substrate surface to be plated; selectively illuminating the coated substrate surface with laser light to ablate a selected area of the strippable coating and

activate an underlying region of the substrate surface exposed by the ablation of the strippable coating; contacting the substrate surface with seeding particles for electroless plating, so that seeding particles adhere preferentially to the activated region of the substrate surface; and electrolessly plating the substrate surface, whereby the seeded areas of the substrate surface are selectively plated.

In one embodiment of the invention, the coating is stripped from the polymer surface after the step of seeding the surface, thereby removing any undesired seeding particles on the coating prior to plating.

In another embodiment, the coating is stripped from the polymer surface after the step of plating the surface, thereby removing any undesired plating with the coating.

In another aspect, the invention provides a substrate formed with circuitry which includes vias having a non-circular cross-section, thereby enabling the density of the substrate circuitry to be increased.

In yet a further aspect, the invention provides a method of re-mapping a wafer, comprising using a laser to re-configure an existing circuit pattern on a surface of the wafer.

In order that the invention may be readily understood embodiments thereof will now be described in more detail, by way of example, with reference to the accompanying drawings, in which:

Figures 1(a) to 1(h) are diagrammatic illustrations of the steps in a plating method embodying the present invention;

Figures 2(a) and 2(b) illustrate a known method of forming vias on a polymer substrate;

Figures 3(a) and 3(b) illustrate a method of forming vias using the method of the present invention;

Figures 4(a) and 4(b) illustrate the formation of non-circular vias using a method embodying the present invention; and

Figures 5(a) to 5(d) illustrate a method of re-mapping a semiconductor wafer employing a method embodying the invention.

The Figures 1(a) to 1(h) of the drawings show the various stages of a method embodying the invention for plating a substrate 1, for example a semiconductor substrate, provided with a layer 2 of an aromatic polymer, such as a polyimide, a polycarbonate or an epoxy, on a surface 1a of the substrate to be plated.

As shown in Figure 1(a), in a first step of the method, a thin coating 3 of a strippable, non-aromatic polymer is applied to the aromatic polymer substrate layer 2. In this context, the term “strippable” is used to denote a material that can subsequently be easily removed, for example by immersion in a solvent, without significantly damaging the underlying aromatic polymer surface.

Figure 1(b) illustrates a second step of the method in which light 4 from a laser (not shown) is used to selectively activate the aromatic polymer. In this procedure, the laser light 4 first ablates the coating 3 over a selected area of the

aromatic polymer layer 2 to expose the layer 2 and then activates the exposed aromatic polymer surface. During activation of the aromatic polymer, the laser power is reduced below the threshold power for ablation of the aromatic polymer and the laser light is directed at the area to be activated until the area in question turns or begins to turn black. In the course of activation, the aromatic polymer surface is not only roughened, but is also chemically altered, causing a change in its surface charge. If require, and as shown in Figure 1(b), the aromatic polymer may also be ablated to a desired depth before activating the surface of the aromatic polymer, thereby producing a recess 2a with an activated surface 5 in the surface of the aromatic polymer layer 2 as shown in Figure 1(c).

For simplicity, Figures 1 (a) to 1(c) only show the activation of a single region of the aromatic polymer layer but it will be appreciated that any desired number of discrete areas or pattern of interconnected areas may be selectively activated by directing the laser light appropriately.

Once the desired surface areas of the aromatic polymer layer 2 have been activated, the substrate may be selectively plated as will now be described with reference to Figures 1(d) to 1(h).

Referring to Figure 1(d), to achieve plating of the selectively activated areas of the aromatic polymer layer 2, the substrate is first immersed in a seeding solution for electroless plating, containing polymer-stabilised catalytic particles such as polyvinylpyrrolidone (PVP) stabilised palladium particles. In this environment seeding particles 6 (shown on a grossly exaggerated scale in Figure 1(d)) from the seeding solution are preferentially adsorbed on the activated surface areas of the aromatic polymer. Potentially, however, stray

seeding particles 6a may adhere to the non-activated surfaces of the polymer coating 3.

In one variant of the method embodying the invention, the substrate with its polymer coating 3 still in place is then immersed in an electroless plating bath to form a thin layer 7 of metal on the seeded areas of the surface, see Figure 1(e). Again, whilst the metal layer 7 will be preferentially deposited on the heavily seeded activated areas of the aromatic polymer, some stray plating 7a may form on the polymer coating 3 at the sites of the stray seeding particles 6a. Prior to immersion in the electroless-plating bath, the substrate may be rinsed in ultra pure water and/or possibly subjected to ultrasound cleaning to remove stray seeding particles which are only weakly adhering to the non-activated regions of the substrate.

In the following step of the method, the polymer coating 3 is stripped from the surface of the aromatic polymer. In general, the removal of the coating may be achieved by immersion in a suitable solvent but it is envisaged that any stripping method which does not significantly damage the aromatic polymer may be used. Any stray plating 7a adhering to the strippable coating 3 is removed with the coating, leaving only the plating 7 on the activated regions of the aromatic polymer as shown in Figure 1(f).

As shown in Figure 1(g), a further layer of metal may, if required, then be deposited on the initial plating layer 7 by electroless-plating or by electroplating to form a thicker metallisation 8.

Finally, if desired, the exposed surface 9 of the metallisation 8 may be planarised as shown in Figure 1 (h).

In another variant of the method embodying the invention, the polymer coating 3 is stripped from the substrate after the seeding step and before the initial electroless-plating step. In this variant of the method, any stray seeding particles adhering to the surface of the coating 3 are removed together with the coating, so that plating only forms on the activated areas of the aromatic polymer during the subsequent electroless-plating step.

A plating method embodying the present invention finds particular application in the fabrication of landless vias and this aspect of the invention will now be described with reference to Figures 2 to 4 of the drawings.

Referring to Figures 2(a) and 2(b), present practice requires the surface circuitry 10 on printed circuit boards (PCBs) and flexible substrates to be patterned separately from the drilling and metallisation of any vias 11. In a typical process, the surface circuitry 10 is patterned first as shown in Figure 2(a), leaving lands 12, i.e. large circular areas, through which the vias 11 are subsequently drilled as shown in Figure 2(b). Such lands 10 are necessary for alignment during the drilling of the vias 11.

Using a plating method embodying the present invention it is possible to drill the vias and activate the surface and vias in one step. It is also possible to metallise the vias and surface circuitry in one step. Thereby eliminating the need for alignment between steps and obviating the need for lands. Without lands denser circuitry is possible.

Figure 3(a) shows a substrate to be plated by a method embodying the invention after the drilling of the vias and activation of the circuitry and vias,

while Figure 3(b) shows the same substrate after plating. Thus, Figures 3(a) and 3(b) show vias 21 drilled in a coated substrate 22 and then laser activated for seeding together with surface circuit patterns 20. The activated surfaces of the vias 21 and the circuit patterns 20 are then selectively plated as described above with reference to Figures 1(d) to 1(h).

A further development is illustrated in Figures 4(a) and 4(b), which are respectively a plan view and a cross-sectional view of a substrate formed with non-circular vias. In this further development, non-circular vias, such as slot-shaped vias 31, are formed and plated together with circuit patterns 30 by the method embodying the invention. This allows the circuitry to be made even more dense.

Figures 5(a) to 5(d) illustrate another application of the invention, in this case to the re-mapping of a wafer. Referring to Figure 5(a) this first involves applying an aromatic polymer layer 51 to the wafer 50 to be re-mapped and covering the layer of aromatic polymer with a strippable coating 52 of a non-aromatic polymer. A laser is used to ablate through the strippable layer 52 and to drill vias 53, see Figure 5(b), the laser power then being reduced to activate the exposed surface 54 of the aromatic polymer layer 51. The activated surface is next seeded and the strippable coating is removed, Figure 5(c). The seeded surface is finally plated in an electroless bath to form the re-mapping plated circuitry 55 which is shown in finished form in Figure 5(d), in which the new vias 53 and circuit pattern 55 on the aromatic polymer layer 51 re-map the wafer into the desired configuration. Figure 5(d) also shows a solder ball 57 for connecting the re-mapped circuitry to a substrate (not shown) and a solder mask 56 for protecting the surface of the remapped wafer 50 during soldering, the mask 56 having an aperture receiving the solder ball 57.

The method of the present invention can also be used to fabricate fine-line circuitry by using the laser light to ablate completely through the strippable coating and partially through the layer of aromatic polymer to produce a channel. The bottom of the channel can then be activated by the laser for seeding. Once the bottom of the channel has been seeded and the strippable coating has been removed, plating will proceed upwards from the bottom of the channel. Unlike plating on a flat surface, the plating will thus be confined and the plated metal will simply grow upwards and not upwards and sideways as it would on a flat surface. This laser ablation of channels together with the strippable coating on the surface on the aromatic polymer layer enables the production of extremely fine-line circuitry embedded in the polymer layer.

A further application of a method embodying the present invention is in the field of integrated resistors. A major requirement in the microelectronics packaging industry is to reduce the bulk of passive circuit components, such as resistors, capacitors and inductors, which commonly occupy up 70% of the surface of a PCB or flex substrate. As a contribution to reducing the bulk of these passive components, a method embodying the present invention provides easy fabrication of integrated resistors by activating, seeding and plating a region on a substrate between two copper interconnects, the seeded region being plated with a high resistivity metal, such as a nickel-phosphorus or nickel cobalt alloy. Such a resistor occupies far less space than a non-integrated resistor.

Using a plating method embodying the invention also facilitates the rapid prototyping of circuit designs. Rapid prototyping is important in the microelectronics industry, since designers need to be able to test their new

designs quickly and easily. Conventional circuit plating methods require a mask which is costly and time-consuming to produce with each new design requiring a new mask. Using a plating method in accordance with the present invention, which does not require a mask, enables rapid and efficient prototyping to be performed.

It is envisaged that a method embodying the invention could also be used to activate, seed and plate non-planar features on a surface, such as bumps, to serve as connectors or probes.

In the present specification "comprises" means "includes or consists of" and "comprising" means "including or consisting of".

The features disclosed in the foregoing description, or the following claims, or the accompanying drawings, expressed in their specific forms or in terms of a means for performing the disclosed function, or a method or process for attaining the disclosed result, as appropriate, may, separately, or in any combination of such features, be utilised for realising the invention in diverse forms thereof.

CLAIMS:

1. A method of plating a substrate material, which when activated by laser light adsorbs seeding particles for an electroless plating process, comprising applying a strippable coating to a substrate surface to be plated; selectively illuminating the coated substrate surface with laser light to ablate a selected area of the strippable coating and to activate an underlying region of the substrate surface exposed by the ablation of the strippable coating; contacting the substrate surface with seeding particles for electroless plating, so that the seeding particles adhere preferentially to the activated region of the substrate surface; and electrolessly plating the substrate surface, whereby the seeded areas of the substrate surface are selectively plated.
2. A method according to claim 1, comprising removing the strippable coating after contacting the substrate surface with seeding particles but prior to electrolessly plating the substrate surface.
3. A method according to claim 1, comprising removing the strippable coating after electrolessly plating the substrate surface.
4. A method according to any one of claims 1 to 3, wherein the substrate material is an aromatic polymer and the strippable coating comprises a non-aromatic polymer.
5. A method according to any preceding claim, comprising using the same laser to ablate the strippable coating and to activate the substrate surface, and reducing the power of the laser for the activation of the substrate surface.

6. A method according to any preceding claim, comprising depositing further metal on the electrolessly plated region of the substrate.
7. A method according to claim 6, comprising depositing the further metal by electroless plating.
8. A method according to claim 6, comprising depositing the further metal by electroplating.
9. A method according to any preceding claim, comprising ablating the substrate material underlying the ablated area of the strippable coating to form a recess in the substrate material before activating the polymer surface.
10. A method according to claim 9, comprising fabricating fine-line circuitry by ablating channels in the substrate material and filling the channels with metal after electroless plating of the activated surfaces of the channels to form circuitry embedded in the substrate material.
11. A method according to any preceding claim, comprising using the laser to ablate the strippable coating, selectively activate the substrate surface and drill a landless via in the substrate material in the same step.
12. A method according to claim 11, wherein the landless via is non-circular.
13. A method according to claim 12, wherein the non-circular landless via is slot-shaped.

14 A method according to any preceding claim, comprising selectively plating non-planar features on the substrate surface.

15 A method according to any preceding claim, comprising forming an integrated resistor by selectively activating and plating a region between two circuit interconnects on the substrate surface.

16. A method according to claim 15, comprising plating the activated region with a nickel alloy to form the resistor.

17. A method according to any preceding claim used to re-map a wafer.

18. A substrate formed with circuitry which includes vias having a non-circular cross-section, thereby enabling the density of the substrate circuitry to be increased.

19. A substrate according to claim 18, including slot-shaped vias.

20. A method of re-mapping a wafer, comprising using a laser to re-configure an existing circuit pattern on a surface of the wafer.

ABSTRACT

“Method of forming selective electroless plating on polymer surfaces”

A method of plating an aromatic polymer substrate comprises: applying a strippable coating of a non-aromatic polymer to a substrate surface to be plated; selectively illuminating the coated substrate surface with laser light to ablate a selected area of the strippable coating and to activate an underlying region of the substrate surface exposed by the ablation of the strippable coating; contacting the substrate surface with a seeding solution containing polymer-stabilised catalytic seeding particles, so that the seeding particles adhere preferentially to the activated region of the substrate; and electrolessly plating the substrate surface, whereby the seeded areas of the substrate surface are selectively plated.

Fig. 1

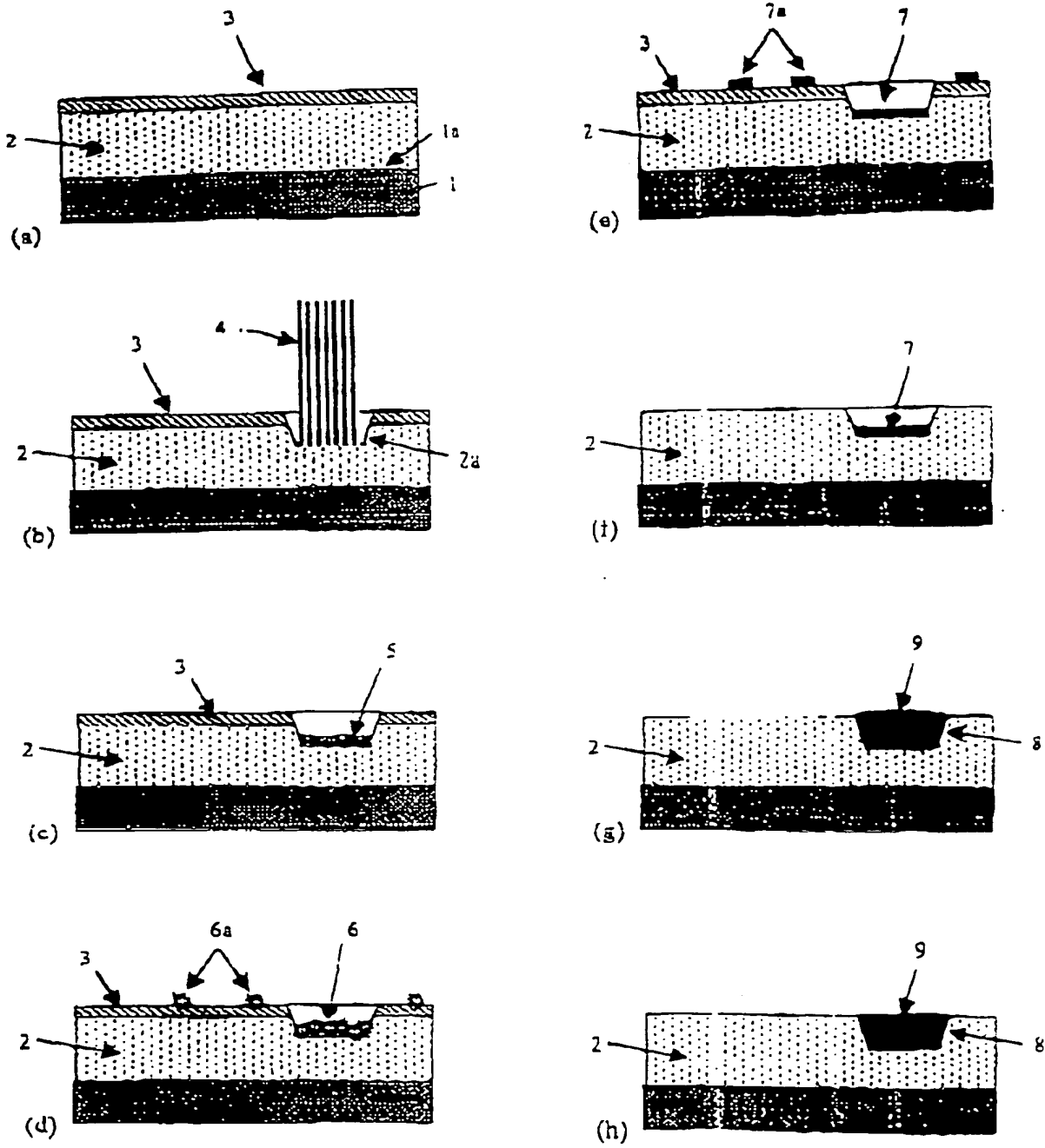


FIGURE 1

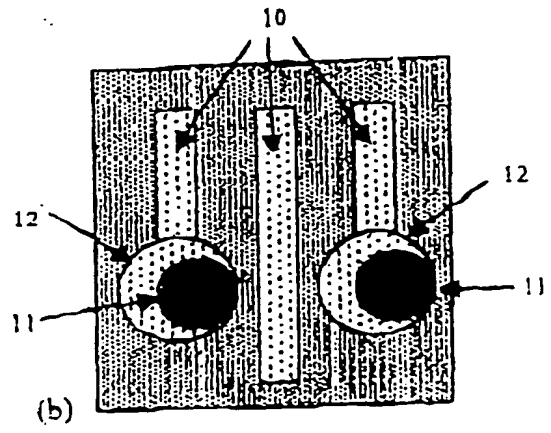
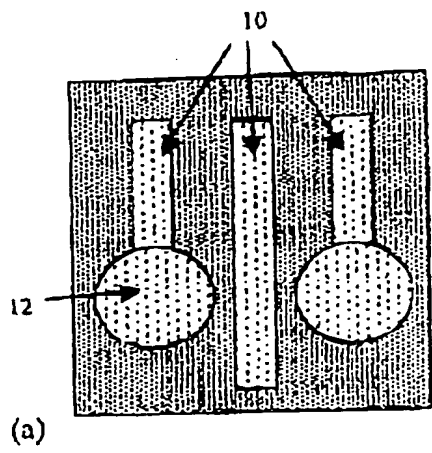


FIGURE 2

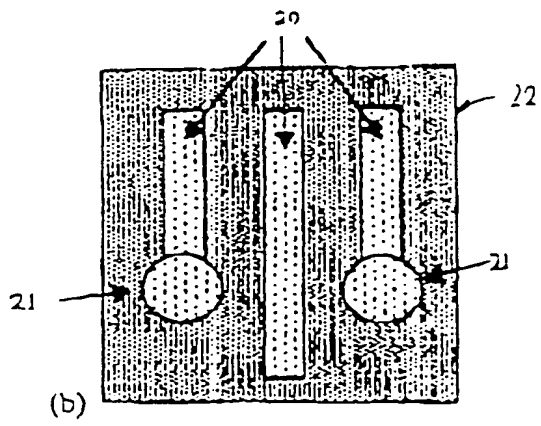
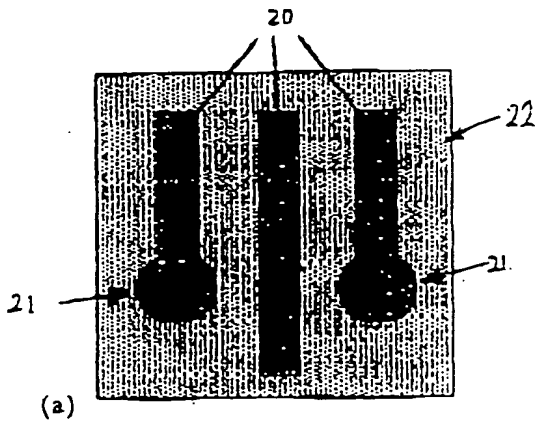


FIGURE 3

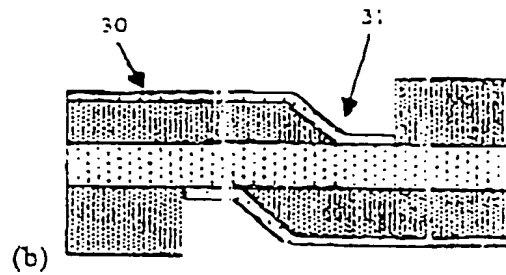
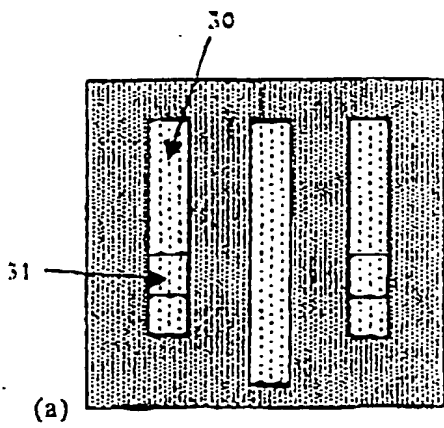


FIGURE 4

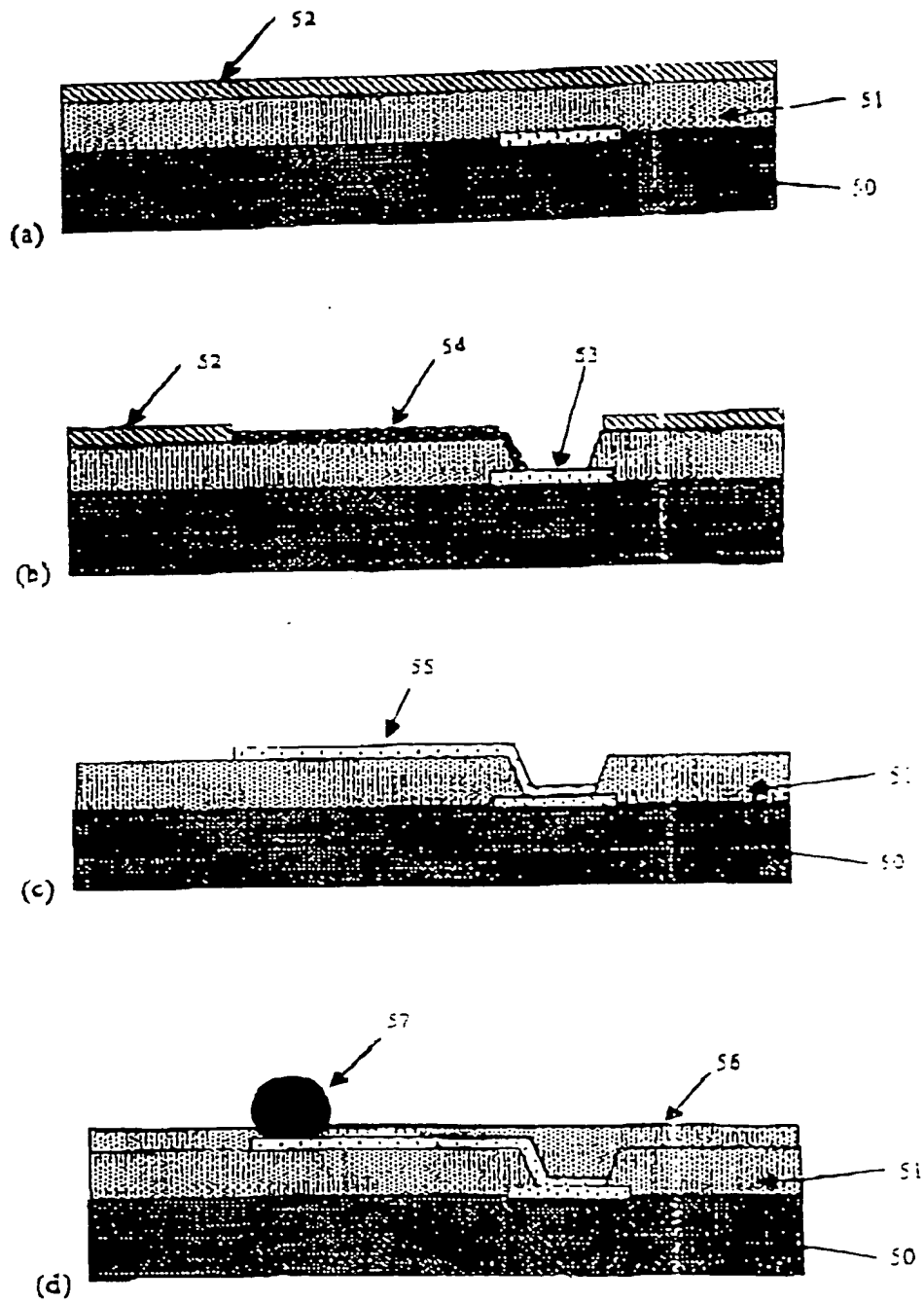


FIGURE 5